# Design, Simulation, and Verification of a Multi-Protocol SerDes

Silicon Creations



# ABSTRACT

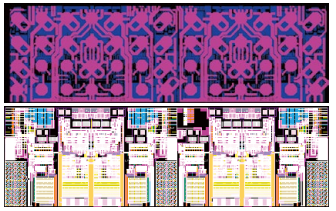
Development of an enterprise-level SerDes PMA reaching over 12Gb/s in TSMC 40LP requires very careful and robust development procedures. Following a brief overview of our products in TSMC technologies ranging from 7nm to 180nm we provide an overview of some the challenges in developing this challenging IP to be taped out in October, and the design simulation methods needed for success.

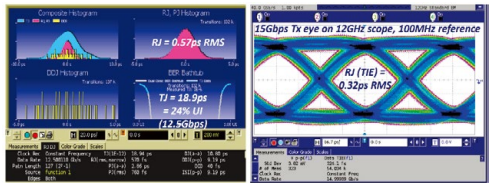
# Design, Simulation, and Verification of a Multi-Protocol SerDes

Jeff Galloway, Andrew Cole, Dr. C.C. Chen, Dr. Ivan Hsiao, Jeff Lumish, Randy Caplan

## Talk Overview

- Summary of Silicon Creations and products at TSMC
- A few challenges faced in designing a 12.7Gb/s Enterprise SerDes in TSMC 40 LP

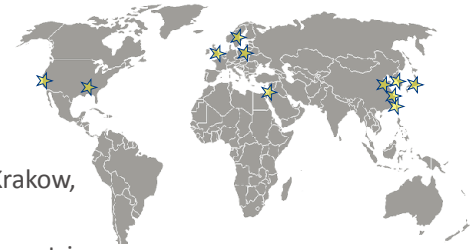







## Corporate Overview

- Analog/Mixed-Signal Silicon IP provider
  - Interface IP including SerDes (today)
  - PLLs & precision timing IP
- Founded in 2006
  - Privately held & self-funded
  - Profitable since founding, growing
- Design centers in Atlanta, GA and Krakow, Poland
- >110 customers from 15 different countries
- Over 100 mass production IPs at TSMC from 16nm to 180nm, proven PLLs in 10nm
- Customers in nearly all electronics niches
  - Consumer / mobile, automotive, IoT, industrial, aerospace





## Find our IP in TSMC ONLINE

**IP Comparison**

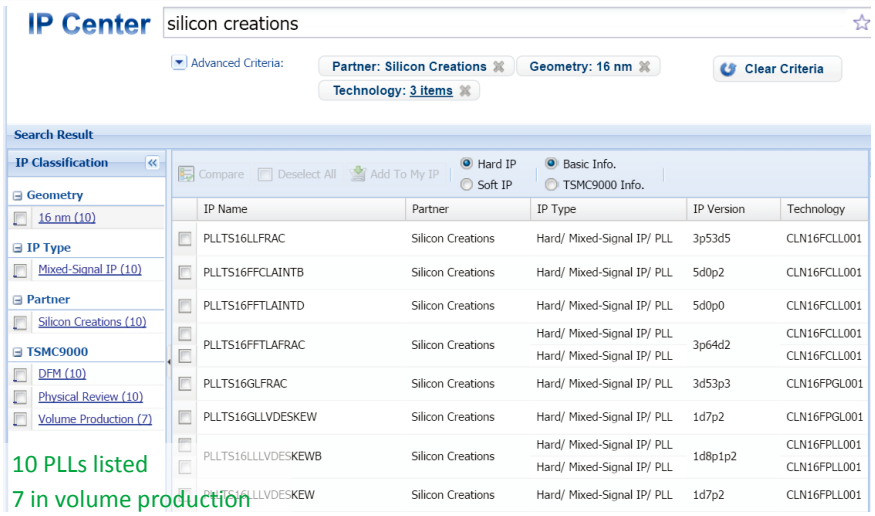
| IP Name | PLLTS40LPFRAC | PLLTS28HPMLVDESKEW | PLLTS28HPMFRAC | PLLTS16GLFRAC | PLLTS16FFCLAINTB |
|---|---|---|---|---|---|
| Partner Name | Silicon Creations | Silicon Creations | Silicon Creations | Silicon Creations | Silicon Creations |
| Contact Me | Contact Me | Contact Me | Contact Me | Contact Me | Contact Me |
| Geometry | 40 nm | 28 nm | 28 nm | 16 nm | 16 nm |
| Technology | CLN40LP | CLN28HM | CLN28HM | CLN16FPGL001 | CLN16FCLL001 |
| IP Category | Hard | Hard | Hard | Hard | Hard |
| IP Type | Hard/ Mixed-Signal IP/ PLL | Hard/ Mixed-Signal IP/ PLL | Hard/ Mixed-Signal IP/ PLL | Hard/ Mixed-Signal IP/ PLL | Hard/ Mixed-Signal IP/ PLL |
| IP Description | Wide range, programmable fractional-N PLL | 0.9V/1.8V,Core voltage De-Skew PLL | 0.9V/1.8V,Programmable Fractional-N PLL | 0.8V/1.8V,Programmable Fractional PLL | 0.8V/1.8V,Low Area Core Voltage Integer PLL |
| Volume production | 18/254667 | 14/37702 | 67/452921 | 15/154976 | 1/5477 |

| | | | | | |
|---|---|---|---|---|---|
| Process: | 40LP | 28HPM/C/C+ | 28HPM/C/C+ | 16FF+GL | 16FFC |
| Tapeouts: | 18 | 14 | 67 | 15 | 1 |
| Wafers: | 255k | 37k | 453k | 155k | 5.4k |

… Over 115 chips and over 900k wafers in top 5 products… most chips have multiple PLLs

… Over 16 production tapeouts in 16nm including production in 16FFC

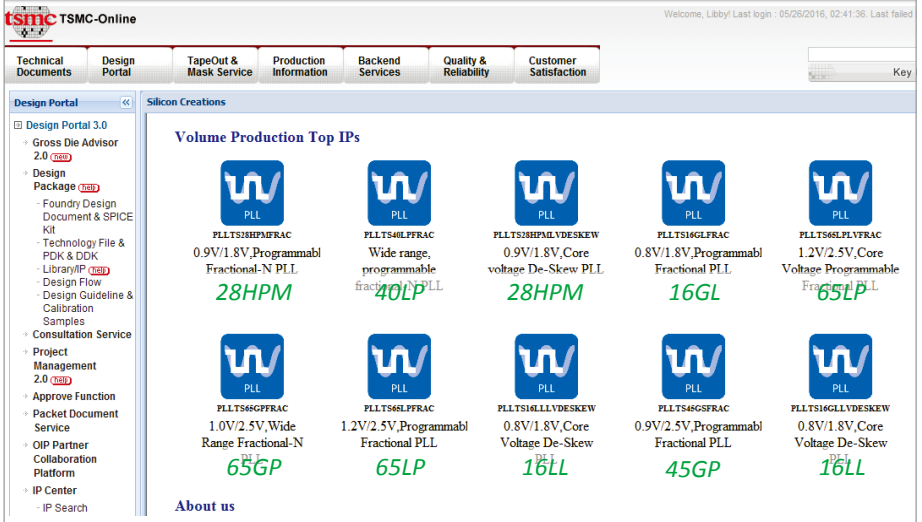
# 16FF+/16FFC IP Listings




10 PLLs listed
7 in volume production



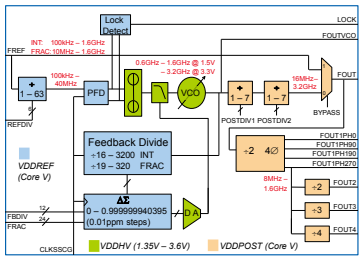
# IP Center - Partner Hub






# Products (1) - PLLs

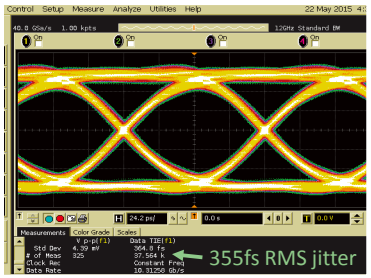
- Production at TSMC from 16nm to 180nm, proven in 10nm, collaborating at 7nm
- Very high production volumes … E.g. TSMC 28nm:
  - >67 production chips, >450k wafers
  - Production runs over 45,000 wafers
  - Up to 17 PLLs per chip
  - Robust design and good QA relies on trustworthy models and PDK
- Other PLL IPs at TSMC include
  - Low Jitter (for AFE, SerDes)
  - µW / 32kHz reference (“IoT”)
  - Multiphase, de-skew

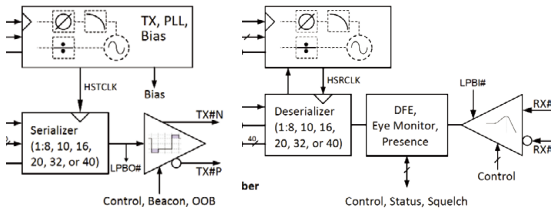


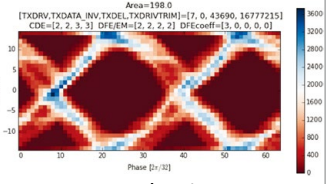



# Products (2) - SerDes

- Focus of today’s talk Multiprotocol “Enterprise” SerDes PMA covering 250Mb/s to 12.7Gb/s
- Proven in 28nm
- TSMC 40 LP test chip taping out in October



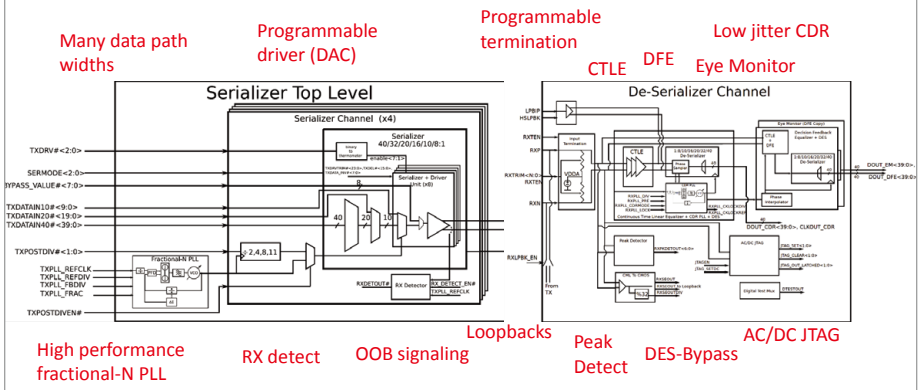



Eye Mon, Adaptive Eq.

# SerDes PMA

- Enterprise SerDes has many analog/mixed-signal blocks
  - A lot of SPICE level verification is needed!
  - Mixed mode Verilog is essential for speed and full coverage






# SerDes simulation challenge

- SerDes and PLL time scales present a challenge for simulation

| | |
|---|---|
| Jitter requirements … | ~100fs |
| Bit rates … | ~100ps |
| Word rates … | ~10ns |
| AC coupling time constant … | ~1µs |
| PLL lock time … | ~50µs |
| Link behavior … | ~1ms |

10 orders of magnitude!



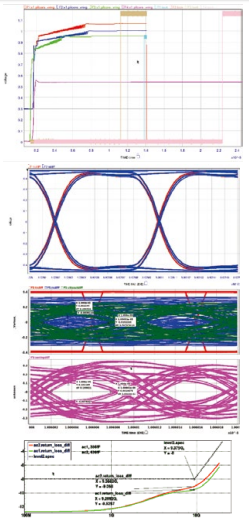
# PLL SPICE simulation history

- 1996
  - Pre-set loop filter voltage & PFD state
  - See if loop is going in the right direction
  - Wait 3 weeks for a schematic lock simulation
- 2001
  - 1 week for a schematic lock simulation
- 2006
  - 3 days for a schematic lock simulation
- 2011
  - A few days for an extracted lock simulation
- 2016
  - Kick off a bunch of extracted lock simulations, check the results the next morning! ☺
  - Complex FinFET models, and thinner metal require RC extraction and intelligent netlist reduction for success, reliability & ageing… more simulations



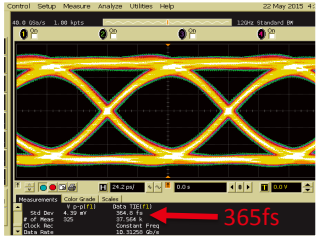
# Example SerDes Simulations

- PLL locking
  - 24µs of simulation time @ 12Gb/s
- TX eye diagram
  - 1000's of bits
  - time step accuracy of <<1ps
- DFE/CTLE + channel
  - Including S-parameter models of 36" channel & package + AC coupling on PCB
- Frequency domain return loss
  - Including S-parameter models



# Jitter – a key parameter

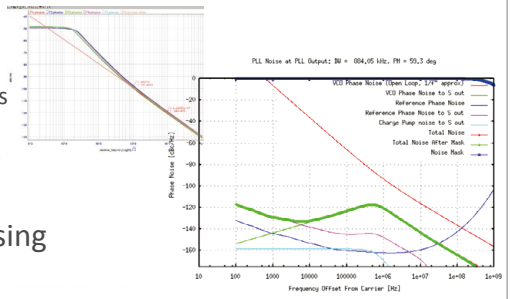
- Jitter is difficult, but critical, to simulate!
- Must understand and analyze many sources
  - Thermal and 1/f noise, locking states, power supply network, supply noise, package, …
- Both long term and short term jitter must be well understood, modeled, and simulated for a low-jitter transmit eye!



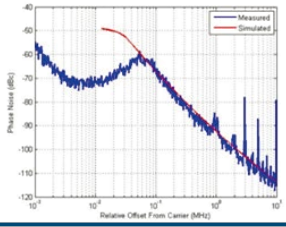



# Frequency Domain Analysis

- VCOs simulated using PSS/P-noise
  → VCO phase noise & contributors
- Add transfer functions to SerDes output
- Phase noise integrated to calculate long-term jitter using MatLab



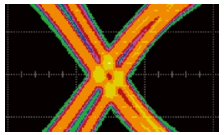
- Verified using transient noise → silicon accurate results
  *"Silicon-Accurate Mixed-Signal Fractional-N PLL IP" – TSMC OIP, San Jose 2012*

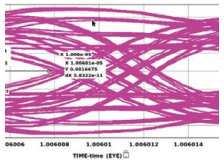




# Inter-symbol Interference

- ISI comes from
  - Bandwidth limitations
    - I/O & ESD capacitance, channel loss
    - Tradeoffs with power
    - … Optimization with inductors & matching structures
  - Multipath propagation
    - Parasitic coupling paths via supplies, substrate
- Many simulations
  - Full R-C extraction with careful netlist reduction
  - PCB + S-parameter package models essential
  - Fixed short patterns for DCD, ½ and ¼ rate artifacts
  - PRBS 2^7-1 and 2^15-1 for eye diagrams, AC coupling, DC feedback

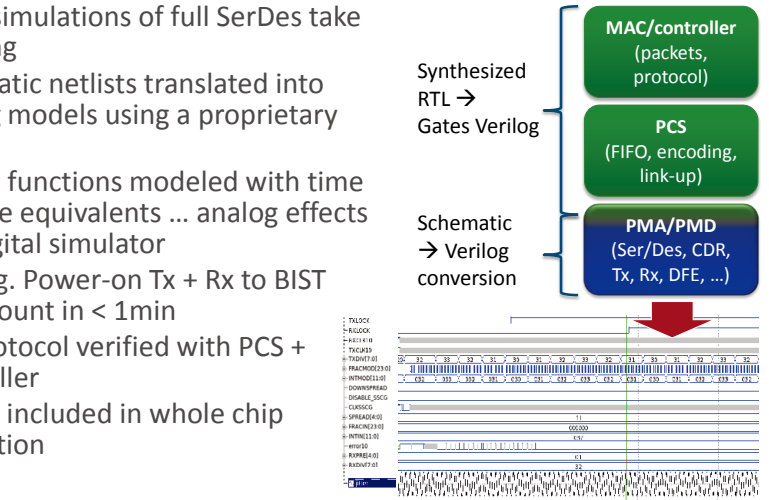






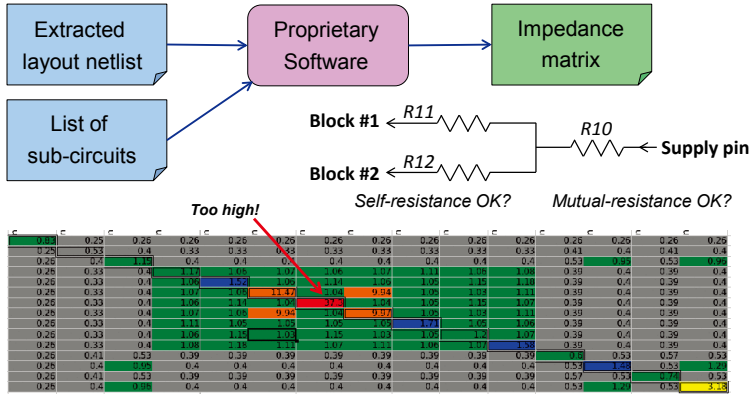
# Verilog Simulations

- SPICE simulations of full SerDes take too long
- Schematic netlists translated into Verilog models using a proprietary flow
- Analog functions modeled with time discrete equivalents … analog effects in a digital simulator
- Fast E.g. Power-on Tx + Rx to BIST error count in < 1min
- Full protocol verified with PCS + Controller
- Can be included in whole chip simulation



# Supply integrity

Impossible to simulate all coupling effects via supplies (complex network in layout … 7+ metal layers and multiple paths). Need automation to identify potential trouble spots.






# Summary

- Silicon Creations has collaborated with TSMC from 7nm to 180nm
  - Reliable extraction and trustworthy models are essential for time to market – TSMC provides
  - Find our IP in TSMC Online – IP Search or Partner Hub
- SerDes/PLL simulation isn't easy!
  - Diverse time scales and many different circuits … but with care 12.5Gbps is possible in TSMC 40LP
- SerDes simulation has come along way in the last 20 years
  - Basic functionality can now be checked "over night"
- Jitter and phase noise simulation is possible with silicon accurate results
- The effect of interconnect can be checked on a large scale
  - Judgment is needed to balance simulation time and accuracy
- Multiple simulation methods are required
  - VerilogD is needed at the system level, but accurate analog models are needed to capture jitter PLL behavior
  - Supply integrity is critical, not all effects can be simulated

Thank you!